IN THE SPECIFICATION:

Page 3, the paragraph appearing in lines 3-4 has been amended as follows:

--Hereinafter, the semiconductor device including an alternating conductivity type drain drift layer will be referred to as the super-junction semiconductor device.--

Pages 3-4, the paragraph spanning these pages has been amended as follows:

--The conventional guard ring formed for controlling the depletion electric field on the peripheral surface portion of the device or the conventional field plate structure formed for controlling the depletion electric field on the insulation film may be used to obtain a high local breakdown voltage in the peripheral region of the device adjacent to the outermost p-type base region 13. It is difficult, however, to optimize the integral structure integrating the alternating conductivity type drain drift layer 22 for obtaining a higher breakdown voltage and the conventional guard ring or the conventional field plate for obtaining a certain local breakdown voltage in the peripheral region of the device. In other words, it is difficult to correct the depletion electric field by an external means added from outside such as the integral structures described above. The reliability of semiconductor device having such an external means for correcting depletion electric field is not high. Since the deep portion of the device spaced apart from the guard ring is not depleted, the local breakdown voltage in the peripheral region of the device is not so high as the breakdown voltage in the drain drift layer 22. Therefore, the conventional guard ring or the conventional field plate is not effective to provide the entire device structure with a high breakdown voltage nor to fully utilize the functions of the alternating conductivity type drain drift layer. It is also necessary to employ the steps of forming masks for

realizing the integral structure, implanting impurity, driving the implanted impurity atoms, depositing metal films, patterning the deposited metal films and such additional steps for manufacturing the super-junction semiconductor device.--

Page 6, the paragraph appearing in line 13 has been amended as follows:

--Fig. 1(b) is the vertical cross sectional view along 1(b)-1(b) of Fig. 1(a).--

Page 6, the paragraph appearing in line 22 has been amended as follows:

--Fig. 4(b) is the vertical cross sectional view along 4(b)-4(b) of Fig. 4(a).--

Pages 9-10, the paragraph spanning these pages has been amended as follows:

--Referring to Fig. 1(b), the n-channel vertical MOSFET includes an n^+-type drain layer (n^+-type drain contact layer) 11; a drain electrode 18 in electrical contact with n^+ drain layer 11; a drain drift region 22 including a first alternating conductivity type layer on n^+ drain layer 11; heavily doped p-type base regions (p-type well region) 13a, which constitute an active region of the device, formed selectively in the surface portion of drain drift region 22; a heavily doped n^+-type source region 14 formed selectively in p-type base region 13a; a gate insulation film 15 on the semiconductor chip; a polysilicon gate electrode layer 16 on gate insulation film 15; and a source electrode 17 in electrical contact with n^+-type source regions 14 and p-type base regions 13a through contact holes bored through an interlayer insulation film 19a. The n^+-type source region 14 is formed in the surface portion of [in]the p-type base region 13a, constituting a

double-diffusion-type MOS structure. Although not shown in Figs. 1(a) and 1(b), gate wiring metal films are in electrical contact with gate electrode layers 16.--

Page 10, the first full paragraph has been amended as follows:

--As described below, the first alternating conductivity type layer in drain drift region 22 is a laminate formed by epitaxially growing n-type layers on a substrate (n^+ drain layer 11). The first alternating conductivity type layer includes n drift current path regions 22a and p partition regions 22b. The n drift current path regions 22a and p partition regions 22b extend vertically (in parallel to the thickness direction of the semiconductor chip) and alternately laminated horizontally with each other. In the first embodiment, the upper end of n drift current path region 22a reaches a channel region 12e in the surface portion of the semiconductor chip, and the lower end of n drift current path region 22a is in contact with n^+ drain layer 11. The upper end of p partition region 22b is in contact with the well bottom of p-type base region 13a, and the lower end of p partition region 22b is in contact with n^+ drain layer 11. The width P1 of a pair of n drift current path region 22a and [n]p-type partition region 22b may be much thinner than that of the illustrated pair of n-type drift current path region and [n]p-type partition region. In this case, it is preferable to extend the boundary between n drift current path regions 22a and p partition regions 22b in perpendicular to the horizontal extending direction of p-type base regions 13a.--

Pages 13-14, the paragraph spanning these pages has been amended as follows:

--An n-type surrounding region 24 with low resistance surrounds the side faces of the second alternating conductivity type layer. The n-type surrounding region 24 works as a channel

stopper for preventing inversion layers from being created in the surface portion of the second alternating conductivity type layer. Since the n-type surrounding region 24 covers outer plane 20B, on that the end faces of n^- regions 20a and p^- regions 20b of breakdown withstanding region 20 are arranged alternately, the side faces of the second alternating conductivity type layer are not exposed outside as the dicing planes of the semiconductor chip and the circumferential area of the second alternating conductivity type layer is biased at the drain potential. Therefore, the dielectric breakdown voltage of the device is stabilized and the quality of the device is improved. The n-type surrounding region 24 does not always surround the side faces of the semiconductor chip. The n-type surrounding region 24 may be formed as an isolation means for isolating semiconductor devices in a semiconductor chip [form]from each other.--

Pages 19-20, the paragraph spanning these pages has been amended as follows:

--When the boron concentrations in the first alternating conductivity type layer in drain drift region 22 and the second conductivity type layer in breakdown withstanding region 20 are the same 2×10^{15} cm^{-3}, the breakdown voltage is 880 V at the phosphorus concentration of 2×10^{15} cm^{-3}. When the manufacturing method described above in connection with the first embodiment is employed, an impurity concentration distribution with the maximum concentrations at the diffusion centers is caused. In other words, impurity concentration variations are caused. In the phosphorus concentration range between 70 % and 130 %, the breakdown voltage changes by 400 V. When the boron concentration is low 5×10^{14} cm^{-3}, the breakdown voltage is 880 V at the phosphorus concentration of 2×10^{15} cm^{-3}. And, the breakdown voltage changes by only 20 V in the phosphorus concentration range between 70 %

and 130 %. Under the ideal condition, under that the born concentration and the phosphorus concentration are the same, the breakdown voltage is independent of the impurity concentrations. However, the breakdown voltage is affected by the concentration ratio of the impurities of the opposite conductivity types. As the impurity concentrations are lower, the breakdown voltage is less dependent of the ratio of the impurity concentrations. Considering that the breakdown voltage is constant 880 V irrespective of whether the boron concentration is 2×10^{15} cm^{-3} or 5×10^{14} cm^{-3}, it is concluded that a sufficiently high breakdown voltage higher than the breakdown voltage (880V) of the first alternating conductivity type layer in drain drift region 22 is obtained in the second alternating conductivity type layer in breakdown withstanding region 20. Therefore, the breakdown voltage of the device depends on the breakdown voltage of the first alternating conductivity type layer in drain drift region 22. Even when the pitches of repeating P1 and P2 are the same and the impurity concentrations in the first and second alternating conductivity type layers are the same, the strength of the depletion electric field in the second alternating conductivity type layer is lower than the strength of the depletion electric field in the first alternating conductivity type layer. The strength of the depletion electric field is lower in the second alternating conductivity type layer than in the first alternating conductivity type layer due to the extra length, by that the curved electric line of force extending from the well side face of p-type base region 13a to n^+ drain layer 11 is longer than the straight electric line of force extending from the well bottom face of p-type base region 13a to n^+ drain layer 11. Since a breakdown voltage higher than that in drain drift region 22 is obtained for breakdown withstanding region 20 by forming breakdown withstanding region 20 of an alternating conductivity type layer even when drain drift region 22 is formed of an alternating conductivity type layer, the structure of the

first alternating conductivity type layer in drain drift region 22 is optimized easily, the design freedoms for designing a super-junction semiconductor device is increased, and, therefore, the development of the super-junction semiconductor device is facilitated.--

Page 43, the second full paragraph has been amended as follows:

--The vertical super-junction MOSFET according to the seventeenth embodiment is an improvement of the MOSFET according to the third embodiment shown in Figs. 6 and 7. In the MOSFET according to the third embodiment, pitch of repeating P2, at that a pair of the p-type region and n-type region is repeated in breakdown withstanding region 220, is narrower than pitch of repeating P1, at that a pair of p partition region 22b and n drift current path region 22a is repeated in drain drift region 22. Since there exists a sudden gap between the widths of the outermost partition region 22bb of drain drift region 22 and the innermost n region 20aa of breakdown withstanding region 220, imbalance is caused between the charge amounts in the outermost partition region 22bb and the innermost n region 20aa. Due to the charge imbalance, a high electric field strength is caused across the boundary between the outermost partition region 22bb and the innermost <u>n</u> [n]region 20aa and it is difficult for the MOSFET according to the third embodiment to exhibit a high breakdown voltage.--